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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,581	06/26/2003	Brian King Flachs	AUS920020595US1	5119

7590 02/23/2006

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EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,581	FLACHS ET AL.	
	Examiner	Art Unit	
	James Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003 and 27 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☒ Claim(s) *8,12 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 8 is objected to because of the following informalities:

Claim 8 recites: "...placing the a processor..." on page 9, line 14. Claim 8 preamble introduces a "multiprocessor system" comprising a "plurality of processors." Examiner asserts applicant intended claim to read "...placing a processor..." Please change. Appropriate correction is required.

Applicant is advised that should claims 12 and 14 be found allowable, claim 14 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-11, 13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Pessolano (U.S. Patent Publication No. 2004/0268091 A1).

As to claim 1, Pessolano discloses a method of conserving power in a multiprocessor device including a plurality of PUs (processor units) (execution units 160 a-d), comprising the steps of: providing a plurality of blocking channels (dispatch units 144 a-d) associated with a like plurality of PUs (Pessolano discloses a system [100] wherein the functional units [144] in conjunction with control unit [148] and data communication bus [142] to "switch off" the associated execution units [160]; paragraphs 53 and 59); setting a PU (160) to a sleep mode (switched off) when the channel is blocked (via 144) for the operation the processor is attempting (paragraph 59); and returning a PU to normal power conditions when a given type of channel event occurs (paragraph 58, lines 14-17).

As to claim 2, Pessolano discloses a method of conserving the use of electrical energy in a computer processor, comprising: providing a mechanism for blocking transactions (dispatch units 144 a-d); and placing the processor into a low-power state (Pessolano discloses switching off various execution units [160] to achieve lower power consumption; paragraph 58, lines 1-4) when a blocked transaction exists (paragraph 59).

As to claim 3, Pessolano discloses a method wherein the transactions are program instructions and the method comprises the additional steps of: providing a depository channel (register channels 120 a-d) for instructions internal to the processor (Pessolano discloses one of the execution units [160] signaling the control unit [148] at the end of a loop execution which then restores registers [120] to continue instruction process; paragraph 60, lines 1-12); and providing a depository blocking channel (120) for instructions external to the processor (Pessolano discloses a data communication bus [110] which fetches instructions from an instruction memory [not shown] which, as is known in the art, may be fetched from external

random access memory that holds program instructions; paragraph 16, lines 12-20 and paragraph 57, lines 1-6).

As to claim 4, Pessolano discloses a method wherein blockings transactions are channel read or channel write instructions (Pessolano discloses program instructions being fetched from instruction memory. This, as is known in the art, can consist of either memory read or memory write instructions.).

As to claim 5, Pessolano discloses a method wherein channel state is maintained with a channel (transaction pending) count (Pessolano discloses one of the execution units [160] signaling the control unit [148] at the end of a loop execution which, as is known in the art, involves a conditional count; paragraph 60, lines 1-12).

As to claim 6, Pessolano discloses a method wherein the processor is reawakened (reactivated) when the environment performs a transaction that removes the block causing the blocked transaction (Pessolano discloses reactivating an execution unit [160] when a stall is lifted; paragraph 59).

As to claim 7, Pessolano discloses a method wherein: the processor is part of a multiprocessor system (100) (paragraph 53); and the blocked transaction is caused in awaiting a response from another processor of the multiprocessor system (Pessolano discloses one of the execution units [160] signaling the control unit [148] at the end of a loop execution which, as is known in the art, involves a conditional count; paragraph 60, lines 1-12).

As to claim 8, Pessolano discloses a method of conserving the use of electrical energy in a multiprocessor system, comprising: providing a mechanism for blocking transactions (dispatch units 144 a-d) in at least a plurality of processors (execution units 160 a-d) of the multiprocessor

system (100); and placing a processor (160) into a low-power state (switch off) when a blocked transaction exists (paragraph 53 and paragraph 59, lines 1-7).

As to claim 9, Pessolano discloses a method wherein the blocking transaction is caused by the awaiting of a response from the environment (processor system 100) (Pessolano discloses one of the execution units [160] signaling the control unit [148] at the end of a loop execution which then restores registers [120] to continue instruction process; paragraph 60, lines 1-12).

As to claim 10, Pessolano discloses a method wherein: the multiprocessor is on a single chip (paragraph 53); and the environment of a given processor (160) is at least in part on the single chip (100) (paragraph 53).

As to claim 11, Pessolano discloses a method wherein the environment (100) may include another processor (Pessolano discloses that any number of elements may be present; paragraph 54, lines 10-14).

As to claim 13, Pessolano discloses an apparatus for conserving the use of electrical energy in a processor, comprising: blocking channel data storage means (registers 120 a-d) operable to contain data (instructions) for use in connection with the environment outside the processor (execution unit 160) (Pessolano discloses the registers [120] containing instructions fetched from instruction memory; paragraph 57); and low power means (control unit 148) operable to place the processor (160) in a low power mode (switch off) when the blocking channel is at least one of full and empty (Pessolano discloses one of the execution units [160] signaling to the control unit [148] when a loop condition [full or empty count] has been met; paragraph 60).

As to claim 15, Pessolano discloses an apparatus for conserving the use of electrical energy in a processor (execution unit 160), comprising: blocking transaction means (dispatch unit 144) (paragraph 59, 1-7); monitoring means (evaluator 146) operable to place the processor (160) in a low-power state (switch off via registers [120] and dispatch units [144]) when a blocked transaction condition is detected (paragraph 55, lines 1-17).

Claims 12, 14 and 16-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Filippo (U.S. Patent No. 6,983,389 B1).

As to claim 12, Filippo discloses an apparatus for conserving the use of electrical energy in a processor (execution unit 508 or 510), comprising: blocking channel data storage means (instruction scheduler 504) operable to contain data (instructions) for use in connection with the environment outside the processor (Filippo discloses a microprocessor system [500] comprising execution units [508 and 510] responding to instructions fetched from memory or an instruction cache; column 8, lines 39-57); and low power means (activity detector unit 506 or 512) operable to place the processor (508 or 510) in a low power mode (turning clock off to the units) while awaiting a response from the environment (column 8, line 58 thru column 9, line 2).

As to claim 14, Filippo discloses an apparatus for conserving the use of electrical energy in a processor (execution unit 508 or 510), comprising: blocking channel data storage means (instruction scheduler 504) operable to contain data (instructions) for use in connection with the environment outside the processor (Filippo discloses a microprocessor system [500] comprising execution units [508 and 510] responding to instructions fetched from memory or an instruction cache; column 8, lines 39-57); and low power means (activity detector unit 506 or 512) operable

to place the processor (508 or 510) in a low power mode (turning clock off to the units) while awaiting a response from the environment (column 8, line 58 thru column 9, line 2).

As to claim 16, Filippo discloses a method of conserving the use of electrical energy in a computer processor (functional unit 104a or 104b), comprising: normally keeping the processor (104a or 104b) in a low power state (Filippo discloses only clocking the functional unit [104a or 104b] when it is needed which necessitates it normally being kept in a low power state; column 6, lines 17-54); and awakening (clocking) the processor to an active state for only as long as the processor can usefully process data (column 6, lines 17-54).

As to claim 17, Filippo discloses a method comprising, in addition, activation signals (112a or 112b) accompanying the issue of instructions (via input 106) to accomplish the awakening of the processor (column 6, lines 17-54).

As to claim 18, Filippo discloses an apparatus for conserving the use of electrical energy in a computer processor, comprising: a processor (functional unit 104a or 104b) normally maintained in a low power state (Filippo discloses only clocking the functional unit [104a or 104b] when it is needed which necessitates it normally being kept in a low power state; column 6, lines 17-54); and detection means (activity detector/clock control 102a or 102b) operable to awaken the processor (104a or 104b) to an active state (turn clock on) for only as long as the detection means ascertains that the processor can usefully process data (column 6, lines 17-54).

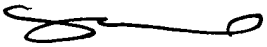
As to claim 19, Filippo discloses an apparatus wherein the detection means (activity detector/clock control 102a or 102b) is responsive to activation signals (input 106) accompanying the issue of instructions to accomplish the awakening of the processor (column 6, lines 17-54).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).



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February 15, 2006